



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/508,846	09/23/2004	Naohito Tomoe	257517US2PCT	8098
22850	7590	09/26/2008	EXAMINER	
OBLON, SPIVAK, MCCLELLAND MAIER & NEUSTADT, P.C. 1940 DUKE STREET ALEXANDRIA, VA 22314			KISS, ERIC B	
			ART UNIT	PAPER NUMBER
			2192	
			NOTIFICATION DATE	DELIVERY MODE
			09/26/2008	ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patentdocket@oblon.com  
oblonpat@oblon.com  
jgardner@oblon.com

<b>Office Action Summary</b>	<b>Application No.</b> 10/508,846	<b>Applicant(s)</b> TOMOE ET AL.	
	<b>Examiner</b> ERIC B. KISS	<b>Art Unit</b> 2192	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 07 July 2008.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                     | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on May 7, 2008, has been entered. Claims 1-20 are pending.

### ***Response to Arguments***

2. Applicant's arguments filed May 7, 2008, have been fully considered but they are not persuasive.

Applicant argues, "The path formed by the TDI line described in TI-BSL is actually transmitting test stimulus *into* the core logic unit . . . ." (Remarks 8). While this statement is mostly correct (there are, in fact, other uses of the TDI line besides transmission of test stimulus), it does not accurately describe the complete boundary scan system disclosed by TI-BSL. In addition to the TDI line, the boundary scan technology consists of individual boundary scan cells (BSCs) placed at each input and output pin of the functional unit. TI-BSL at p. 3. The boundary scan architecture captures inputs and outputs using these BSCs. *Id.*

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

Art Unit: 2192

the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-5, 10-13, and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. App. Pub. 2002/0026553 A1 (Saito) in view of “Product Bulletin: Bondary-Scan Logic,” 1998, Texas Instruments (hereinafter “TI\_BSL”).

Regarding claim 1, *Saito* discloses a signal processor comprising: (1) a plurality of function blocks configured to perform (see, e.g, functional blocks 21 in Fig. 4); and (2) a plurality of dedicated paths configured to transmit debug information for debugging the signal processor, the debug information obtained from respective function blocks of the plurality of function blocks (see, e.g., paragraph [0033]).

*Saito* further discloses a selection multiplex output block connected to the plurality of dedicated paths and configured to receive as input the debug information via the dedicated paths, and output the received debug information (see, e.g., the signal selection means/portion/circuit illustrated in each of Figures 4-9 and 11).

*Saito* fails to expressly disclose at least two of the dedicated paths being provided for one of the plurality of function blocks, said paths configured to transmit input data and output data associated with said one of the plurality of basic blocks, as debug information from said one of the plurality of function blocks to the selection multiplex output block. However, *TI\_BSL* teaches the known technique of boundary scan, where dedicated paths provided by boundary-scan cells are associated with each of the input and output pins of devices on a board (see, e.g., *TI\_BSL* at p. 3). Further, *Saito* alludes to the use of such boundary scan technology, for example, in paragraph [0008] (mentioning use of a “scan chain”). The input and output captured by the input and output boundary scan

cells is further transmitted to a selection multiplex output block (*TI\_BSL* at p. 3 (see the illustrated multiplexers connected to TDO). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate multiple dedicated paths associated with a function block and configured to transmit input data and output data to such a multiplex output block as per the teachings of *TI\_BSL* in order to gain the advantages of fault isolation free from the constraints of physical test access at all phases of product deployment (*TI\_BSL* at p. 3).

Regarding claim 2, *Saito* further discloses: the dedicated output path transmits the debug information serially (see, e.g., paragraphs [0053] and [0054]; compare Fig. 7 (monitor signal [(serial)]) with Fig. 8 (monitor signal (parallel))).

Regarding claims 3 and 4, *Saito* further discloses: the debug information includes input/output data associated with at least one of the plurality of function blocks (see, e.g., paragraphs [0040] through [0042]).

Regarding claim 5, *Saito* further discloses: the debug information is data in an arbitrary size (see, e.g., paragraphs [0061] through [0066], describing the manipulation of the signal size).

Regarding claim 10, *Saito* further discloses: the selection multiplex output block further configured to acquiring an instruction from an outside, selecting the debug information based on the instruction acquired, inputting the debug information selected via the dedicated output path, and outputting the received debug information to the outside (see, e.g., paragraph [0061]).

Regarding claim 11, *Saito* further discloses: the selection multiplex output block selects multiple pieces of debug information based on the instruction, inputs the multiple

Art Unit: 2192

pieces of debug information, multiplexes the multiple pieces of debug information, and outputs multiplexed debug information to the outside (see, e.g., paragraph [0061]).

Regarding claim 12, *Saito* further discloses: the multiple pieces of debug information are acquired from different function blocks (see, e.g., paragraph [0061]).

Regarding claim 13, *Saito* further discloses: the selection multiplex output block performs time multiplexing (see, e.g., paragraph [0061]).

Regarding claim 18, see the disclosure and teachings applied above to claim 1. *TI\_BSL* teaches dedicated paths provided by boundary-scan cells are associated with each of the input and output pins of devices on a board (see, e.g., *TI\_BSL* at p. 3). For reasons stated above, such a claim also would have been obvious.

Regarding claim 19, *Saito* further discloses a memory disposed inside the function blocks (see, e.g., paragraph [0038] (a flip-flop circuit)).

Regarding claim 20, *Saito* further discloses at least one of a DSP, LSI chip, and a FPGA included in the plurality of function blocks (see, e.g., paragraph [0010] (describing a on-chip system LSI)).

5. Claims 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Saito* in view of *TI\_BSL* and JP 09-064811 (*Sony*), as described in the translation submitted by applicant.

Regarding claims 6-9, *Saito* describes a signal processor according to claim 1 (see the rejection above), but fails to expressly disclose its use in a mobile communication system. However, *Sony* teaches the use of a signal processor in such a mobile communication system (see, e.g., paragraph [0015] and Fig. 1). Further, *Sony* teaches the

Art Unit: 2192

specific functional blocks of claims 6-9 in such a mobile communications environment (modulator/demodulator (MODEM) blocks (Claims 7 and 8) (see, e.g., block 5 in Fig. 1); error correction blocks (claims 6 and 9) (see, e.g., paragraph [0019], describing the application of a CRC algorithm)). As the teachings of *Sony* merely represent a specific application (mobile-communication-specific) of a more general signal processing system, such as one with capabilities disclosed by *Saito*, the combination of such known elements would have been within the level of ordinary skill at the time of invention, and therefore, such claims would have been obvious.

6. Claims 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Saito* in view of *TI\_BSL* and U.S. Patent No. 6,684,348 (Edwards et al.)

Regarding claims 14-16, *Saito* describes a signal processor according to claim 1 (see the rejection above), but fails to expressly disclose the incorporation of time information added by a function block and including a plurality of frame counters of different cycles. However, *Edwards et al.* teaches that in a hardware debug (trace) environment, it is known to provide such features (see, e.g., col. 11, line 47, through col. 12, line 42, describing the inclusion of such time/frame data as a timestamp and program counter). As the teachings of *Edwards et al.* describe the known collection of additional time data to enhance debugging in a hardware system, such as one disclosed by *Saito*, the combination of such known elements would have been within the level of ordinary skill at the time of invention, and therefore, such claims would have been obvious.

Regarding claim 17, the CFN and BFN are merely known time frame counters for a prior art WCDMA protocol implementation, and as software incorporating the

Art Unit: 2192

recording of timing information for software is also known (see the teachings of *Edwards et al.* applied above), it would have been within the level of ordinary skill at the time the invention was made to likewise record additional known time information (claim 17 appears to be directed only to the recording of the CFN/BFN as timing information for debugging purposes) as appropriate, and therefore, such a claim also would have been obvious.

### ***Conclusion***

7. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Eric B. Kiss whose telephone number is (571) 272-3699. The Examiner can normally be reached on Tue. - Fri., 7:00 am - 4:30 pm. The Examiner can also be reached on alternate Mondays.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Tuan Dam, can be reached on (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.



Art Unit: 2192

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eric B. Kiss/

Eric B. Kiss

Primary Examiner, Art Unit 2192